UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., an Irish corporation,

Plaintiff,

v.

LG DISPLAY CO., LTD., a Korean corporation; LG ELECTRONICS, INC., a Korean corporation; and SONY CORPORATION, a Japanese corporation,

Defendants.

CASE NO. 6:19-CV-00236-ADA

JURY TRIAL DEMANDED

DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

The "only meaning that matters in claim construction is the meaning in the context of the patent," not in the context of litigation years later when a subsequent owner of the patent may wish the inventors had claimed their invention differently. *Trs. of Columbia Univ. in N.Y. v. Symantec Corp.*, 811 F.3d 1359, 1363 (Fed. Cir. 2016). Defendants' constructions stay true to this basic rule, interpreting the claims in the context of the specification and prosecution history. Solas's constructions, by contrast, violate basic canons of claim construction by interpreting words in a vacuum, by adding words without construing the disputed terms at all, or by interpreting the claims at odds with the intrinsic evidence.

Solas turns a blind eye to what the inventors told the Patent Office to make clear exactly what they did—and did not—invent, because this evidence undermines its litigation-inspired claim constructions. And time and again, Solas ignores the context of the claims and the specification in an attempt to stretch the claims far beyond what the inventors actually invented. Solas frequently insists it is merely proposing "ordinary meanings," but as controlling precedent mandates, the "ordinary meaning" of a claim term is what it means to an ordinary artisan after reading the patent and file history, not by selectively ignoring the intrinsic record. Finally, Solas attempts to buttress its constructions with the conclusory testimony of its expert, Dr. Flasck. But Dr. Flasck's declaration does little more than repeat Solas's brief and add conclusory legal arguments, and the Court may give it little weight. At bottom, Solas attempts to expand the claims of the patents it bought from other companies in ways that war with the inventors' own statements and other intrinsic evidence, while Defendants have proposed constructions amply supported by the specifications and file histories that correctly capture what the inventors told the Patent Office they invented.

II. U.S. PATENT NO. 7,907,137

A. "a gradation current having a current value" (claims 10, 36)

Solas agrees that "a gradation current having a current value" must be a current, and that the current must correspond to a luminance gradation, i.e., light emitting level. Solas's Opening Brief (Dkt. 68, "Sol. Br.") at 6. And the parties and their experts seem to agree that current and voltage are related but different electrical phenomena. Defendants' Opening Brief (Dkt. 67, "Def. Br.") at 2-3; Declaration of Dr. Douglas Holberg (Dkt. 67-2, "Holberg Op. Decl.") ¶¶ 26-28, 32; Sol. Br. at 8 (citing Dkt. 68-2 ("Flasck Decl.") ¶¶ 63-73); Flasck Decl. ¶ 66 (citing separate technical definitions of current and voltage). Yet Solas apparently wants to argue to the jury that because voltage is "inextricably intertwined" with current, if the accused devices generate and supply a ***voltage***, they necessarily satisfy generating and supplying a ***current*** having a ***current*** value. Solas is wrong, both as a matter of claim construction and basic physics.

Defendants' construction expresses what is abundantly clear from the claims, specification, and prosecution history: current means current, not voltage. Indeed, the inventors claimed the use of "voltage" for certain functions, and "current" for others, demonstrating that they knew how to use these terms distinctly in the claims, and they understood their different, if related, meanings. Def. Br. at 5-6; *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000). If, as Solas seems to argue, current and voltage encompass one another simply because they are mathematically related, then it never would make sense to use those terms differently as the inventors chose to do in the claims.

The specification draws marked distinctions between "currents" and "voltages" as well. For example, the inventors made clear to distinguish their "current driven" invention, which provides a "gradation current" to the data line to control luminance, from prior art "voltage driven" circuits that write a "gradation voltage" to the data line to control luminance. *See* Def. Br. at 6-7.

For example, the '137 patent states that the "***present invention*** relates to … being supplied with a ***current corresponding to display data***." '137 patent at 1:18-26; *see also, e.g., id.* at 13:63-67, 15:67-16:5, 20:29-36, 22:4-14, 22:19-24, 22:25-32, 24:2-10, 24:30-37, 28:49-60, 38:10-19, 38:53-58, 56:13-17, Figs. 7, 8, 9, 16 (discussing patent's use of a "gradation current"); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention."). In contrast, the inventors distinguished "conventional" prior art displays supplying "a ***voltage value corresponding to display data***" to control a light emitting operation. '137 patent at 2:34-37 ("gradation voltage"), 3:6-14, Figs. 35 (showing a gradation voltage "Vpix" provided to pixels through a data line), 36 (same). The claims are explicitly limited to a "gradation ***current*** having a ***current value***" to distinguish the claimed inventions from the prior art and its alleged shortcomings. *Id.* at claims 10, 36; *see also id.* at 3:15-41 (shortcomings of voltage gradation).

Solas cites parts of the specification describing a "gradation signal generation circuit" that generates a "non-light emitting display ***voltage*** Vzero" as contradicting Defendant's construction. Sol. Br. at 7-8. Not so. The claim limitation in dispute is a "gradation ***current*** having a current value," and throughout the specification the inventors exclusively refer to the entirely separate "non-light emitting display voltage" as having a "voltage value," but never as having a "current value" or as being synonymous with a "gradation current." '137 patent at 10:52-59, 31:55-57. Indeed, the specification teaches that a "gradation current Idata" and a "non-light emitting display voltage Vzero" are ***alternatives*** that are ***selectively*** applied (i.e., one is provided or the other, never both). *See, e.g., id.* at 10:45-52 ("The gradation signal generation unit (the gradation signal generation circuit) 130 has a function of selectively applying, … ***either of*** a gradation ***current*** Idata and a non-light emitting display ***voltage*** Vzero."), 12:11-12, 13:2-4, 27:1-15, 30:19-21, 31:29-30,

31:55-57, 34:54-57, 35:37-39, 36:36-53, 39:55-57, 51:25-27.

Solas argues that construing this term to clarify that the gradation current is not voltage would exclude the embodiment in Figure 9, where Solas contends a gradation current ***and*** a voltage are generated and supplied by a "gradation signal generation circuit 130" through the data line DL. Sol. Br. at 6-7. Solas is wrong. Consistent with the patent as a whole, Figure 9 on its face explicitly refers only to a "gradation ***current*** Idata" that is output by the gradation signal generation unit, and not a gradation voltage. *Id.* at Fig. 9[1]; *see also id.* at 22:4-9 ("a gradation signal (a gradation current Idata having a negative polarity) output from the gradation signal generation unit 130"), 22:19-25 ("gradation current Idata is drawn via the data line DL"), 22:42-43 ("gradation current Idata (the writing current Iwrt)"). The "voltage" that is applied to "contact point N12," which Solas alleges would be read out by Defendant's construction, is not a gradation signal and is neither generated by the gradation signal generation circuit nor supplied through the data line. Sol. Br. at 6-7. Rather, it is generated by the transistor Tr13 in the display pixel in a "current/voltage conversion function." '137 patent at 24:38-43; *see* Sol. Br. at 8.

If the claims and specification were not enough, the prosecution history is dispositive. Solas should not be heard to argue that its claimed "gradation current" encompasses a voltage because the inventors made the opposite argument to the Patent Office to secure their patent. Specifically, the applicants amended their originally filed claims to add the "gradation current having a current value" term after the examiner rejected the claims as anticipated over Ono. Dkt. 67-6 (Ex. 5) at 2. The applicants then distinguished Ono, which "discloses applying a ***voltage***," as not disclosing "generating and supplying a gradation ***current***" of the claims. Dkt. 67-8 (Ex. 7) at 32; *see also id.*

[1] The '137 patent applies the symbol "I" according to its common usage to refer to current. *See, e.g.*, '137 patent at 22:27-28 ("writing ***current Iwrt*** which corresponds to the current value of the gradation ***current Idata***").

at 33 (stating that "for similar reasons" all of the amended independent claims were distinguished over Ono et al.); Def. Br. at 7. These types of narrowing amendments and arguments more than justify excluding voltage from Solas's claims. *See, e.g., Mangosoft Intellectual Prop. v. Skype Techs. SA*, No. 2:06-CV-390, 2008 U.S. Dist. LEXIS 62281, at *19 (E.D. Tex. Aug. 14, 2008) ("The court concludes that the term 'migrate' does not encompass replication or copying. Rather, it requires a change of the location of a directory part."); *N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1346 (Fed. Cir. 2005) (affirming construction of "generally convex" meaning "***no concave points***."); *RFID Tracker Ltd. v. Wal-Mart Stores Inc.*, 545 F. Supp. 2d 571, 579 (E.D. Tex. 2008), aff'd, 342 F. App'x 628 (Fed. Cir. 2009)) (construing "interrogator/reader" in part as "not a transmitter"); Def. Br. at 8 (additional cases).

Solas next argues that explaining what the gradation current isn't, i.e., a voltage, might confuse a jury because there are voltages that are "related" to the gradation current in the specification. Sol. Br. at 8. There will be no such confusion, as the voltages Solas points to are expressly claimed separately from the disputed term. ***First***, Solas points to the fact that a "gradation current" can be "initially generated by converting a 'digital signal to an analog voltage…" *Id.* Solas omits that the disclosed "digital signal voltage" is not the gradation signal of the claims, but the separately claimed "display data." '137 patent at 10:60-11:3 ("… converting a digital signal voltage ***of each display*** data …"), claims 10 and 36. ***Second,*** Solas argues there is a related "voltage component Vdata corresponding to the gradation signal (display data)," which is claimed separately from the "gradation current" in independent claim 36. Sol. Br. at 8; '137 patent at claim 36 ("adding a voltage component based on the gradation signal to the voltage component based on the compensation voltage"). Here again, the claims are unambiguous in claiming current as the gradation signal, and voltage as a separate and distinct element of the claims—here, a "voltage

component." *CAE*, 224 F.3d at 1317 (different terms presumed to have different meanings).

Finally, Solas tries to support its construction with the declaration of Mr. Flasck. While "[e]xpert testimony also may be helpful, [] an expert's conclusory or unsupported assertions as to the meaning of a term are not." *Fintiv, Inc. v. Apple Inc.*, Case No. 6-18-cv-00372, Dkt. 86 at 3-4 (W.D. Tex. Nov. 27, 2019). Here, and for virtually every other term, Mr. Flasck's declaration essentially parrots, word-for-word, the text of Solas's lawyers' brief and provides no helpful analysis. *Compare, e.g.*, Sol. Br. at 5-8, *with* Flasck Decl. ¶¶ 56-62 (containing essentially identical claim construction arguments and legal conclusions about "lexicography" and "disclaimer"); *see, e.g., DataQuill Ltd. v. Handspring, Inc.*, No. 01 C 4635, 2003 WL 737785, at *4 (N.D. Ill. Feb. 28, 2003) (excluding an expert's declaration that parroted attorney arguments in a brief). Rather, to the extent the Court determines it would be helpful to turn to extrinsic evidence, Dr. Holberg explains the distinctions between generating and supplying current as a data signal corresponding to a light emitting level, as claimed by the '137 patent, rather than voltage, like in the prior art. Holberg Op. Decl. ¶¶ 53-54 (discussing six prior art references, Dkts. 67-22 to 67-27); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1585 (Fed. Cir. 1996) ("prior art documents … are more objective and reliable guides [than expert testimony].").

B. "gradation signal" (claims 10, 15, 36, 37, 39)

The parties agree that the "gradation signal" carries information about a level, or gradation. The sole dispute is whether "a gradation signal" can or cannot be a voltage. It cannot. While Solas protests that Defendants' construction "improperly adds the requirement that the 'gradation signal' must be a 'gradation current,'" it ultimately admits that this is expressly required by the claims themselves: "***the claims require*** generating and/or supplying '***a gradation current … as a gradation signal***." Sol. Br. at 9 (ellipses by Solas).

Solas argues that the Court should ignore this express claim language and expansively construe "gradation signal" to cover voltages because there are "examples of 'gradation signals' that are voltages," not just currents, in the specification. *Id.* This argument fails for two reasons. ***First,*** as discussed above, the patentees were specific and deliberate in claiming a "gradation ***current*** having a ***current*** value … as a gradation ***signal***." That these claims are directed to embodiments that specifically generate a gradation current, not a voltage, is therefore "little cause for concern." *Aug. Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1285 (Fed. Cir. 2011) ("The mere fact that there is an alternative embodiment disclosed in the [specification] that is not encompassed by [our] claim construction does not outweigh the language of the claim"); *see also supra* at Section II.A (explaining that the inventors repeatedly described supplying a "gradation current having a current value" as an alternative to supplying a voltage).

Second, Solas again acts as if its patents come to Court with a clean slate, and ignores the narrowing amendments and express arguments by the applicants during prosecution that now prohibit Solas from trying to broaden "gradation signal" to cover voltages. Sol. Br. at 8. The originally applied-for claims broadly recited a "gradation signal generation circuit which generates a ***gradation signal*** corresponding to a luminance gradation of the display data and supplies ***the gradation signal*** to the display pixel." Ex. 29 at 156.[2] This is effectively the scope Solas asks the Court to grant today. But those claims were rejected by the examiner as anticipated by Ono (discussed *supra* at Section II.A) and, in response, the applicants amended their claims to specify "***a gradation current having a current value*** … ***as a gradation signal.***" Dkt. 67-6 (Ex. 5) at 2. On that basis, the patentees distinguished their invention from Ono that "applied a voltage." Dkt. 67-

[2] Citations to Exs. 28-32, 35 are exhibits to the Declaration of Blake R. Davis in Support of Defendants' Responsive Claim Construction Brief.

8 (Ex. 7) at 32; *see supra* at Section II.A; Def. Br. at 7. Solas now tells the Court the opposite of what its predecessors told the Patent Office: that the claims ***do*** cover voltage as the purported gradation signal. The law does not permit such revisionist history in claim construction.

As the Federal Circuit instructed on nearly identical facts in *North American Container v. Plastipak Packaging*, when "narrowing amendments are made in order to gain allowance over prior art," construing the claims so that they "do not cover certain embodiments disclosed in the patent" is not only appropriate, but may be "compelled." 415 F.3d 1335, 1346 (Fed. Cir. 2005). In that case the patentee amended its claims in view of an obviousness rejection to specify the base of its plastic bottles as "generally convex," and argued that "[t]he shape of the base as now defined in the claims differs from those of [] the [prior art] Dechenne patent, wherein the corresponding wall portions 3 are *slightly concave*." *Id.* (emphasis original). Notwithstanding the fact that two of the figures incorporated within the specification showed concave inner walls—a preferred embodiment—the court found that "the applicant, through argument during the prosecution, disclaimed inner walls of the base portion having any concavity." *Id.* at 1345 (affirming district court's construction of "generally convex" to mean "a majority of convex points along the inner wall and ***no concave points***."). Like the patentees in *North American Container*, the applicants of the '137 patent clearly and unmistakably disclaimed using ***voltage*** as a "gradation signal" in order to distinguish their invention from the prior art. The "inescapable consequence of such an argument is that the scope of the applicant's claims cannot cover" providing a voltage as a "gradation signal." *Id.* at 1345.[3]

[3] Solas's reliance on *Linear Tech. Corp. v. Intl. Trade Comm'n*, 566 F.3d 1049, 1059–60 (Fed. Cir. 2009) and *Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1367 (Fed. Cir. 2008) is misplaced, as there were no relevant amendments or arguments made during prosecution distinguishing the claims from prior art. *See* Sol. Br. at 5.

C. "generates, as the gradation signal, a non-light emitting display voltage having a predetermined voltage value" / "a non-light emitting display voltage having a predetermined voltage value for allowing the optical element to perform a non-light emitting operation is generated as the gradation signal" (claims 15, 39)

As described above, the "gradation signal" limitation in independent claims 10 and 36 is susceptible to one reasonable interpretation, which is that it is limited to a "gradation current" and is not a gradation voltage.[4] The problem is that after amending the independent claims to narrow them to current gradation signals only, the applicants failed to make a corresponding change to the dependent claims. Dependent claims 15 and 39 still refer to a gradation signal as "a voltage" as a relic of the prosecution history and a drafting error that renders them indefinite. Def. Br. at 9-10.

In an attempt to salvage the validity of these claims, Solas makes three flawed arguments. ***First,*** Solas argues that the specification discloses that "gradation signals" can be generated as "a gradation current" or a "non-light emitting display voltage." However, as discussed *supra* at Section II.A and II.B, (1) the independent claims are expressly limited to using a gradation current and (2) the applicants disclaimed using a gradation voltage as an alternative.

Second, Solas asserts that the "gradation signal" in independent claims 10 and 36 is for "light-emitting operations," and in dependent claims 15 and 39 the "gradation signal" is for non-light emitting operations. But to secure their patent, the applicants broadly argued that Ono's "applying a voltage … does not disclose generating and supplying a gradation current as a gradation signal," and never qualified or limited their disclaimer to "light-emitting operations" as Solas now contends. Dkt. 67-8 (Ex. 7) at 32. Nor could they have, because before the applicants

[4] Solas falsely claims that Defendants were "improperly reserved" in explaining why these claims were indefinite. When the parties' counsel met and conferred, Defendants expressly informed Solas that the claims were nonsensical in view of the applicants' amendments to independent claims 10 and 36 and related arguments in prosecution.

amended the claims, the examiner found that Ono anticipated the requirement of a "***non-light emitting*** display voltage having a predetermined voltage value." Ex. 30 at 8.

Third, Solas proclaims that "any gradation signal would have a current component and some voltage value—and the two items are inextricably and mathematically intertwined." Sol. Br. at 13. This now familiar argument remains unsound. Current and voltage are different, even if related, and the applicants themselves amended their claims to rely on that distinction to secure its claims. Moreover, Solas's "intertwined" theory was conspicuously absent from the arguments the applicants made to the Patent Office to distinguish the prior art's use of voltage gradation signals, and the totality of the intrinsic evidence makes clear that Solas's about-face now should be rejected for the reasons set forth *supra* at Section II.A.

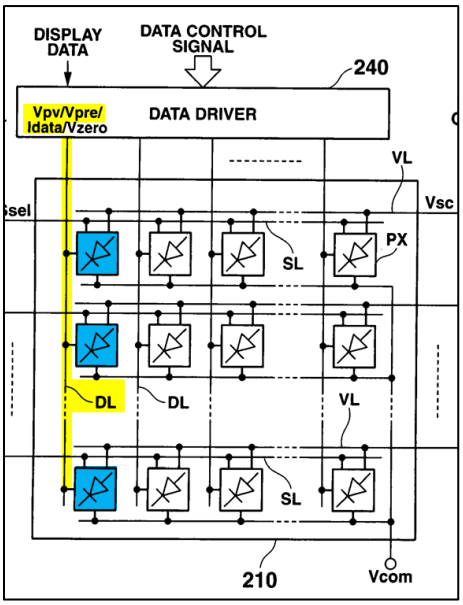
The only construction of "gradation signal" that is consistent with the claim's language, the written description, and the inventors' statements to the Patent Office is that it is limited to "gradation currents," not voltages, rendering dependent claims 15 and 39 invalid. *Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999) ("[I]f the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then ... the claim is simply invalid."); *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357 (Fed. Cir. 1999) (nonsensical claims "must be invalidated, preventing unduly burdening competitors who must determine the scope of the claimed invention based on an erroneously drafted claim.").

D. "through a data line … through the data line … through the data line" (claims 10, 36)

Here, Solas argues against a construction that Defendants have never proposed: "the only substantive dispute," according to Solas, "is whether 'a data line' is limited to 'a ***single*** data line' (as Defendants imply)." Sol. Br. at 14 (emphasis original). Defendants' construction does ***not*** require a "single" data line, and Defendants have never argued or "implied" that it does. The

claims require three functions (supplying, detecting and applying) related to "the display pixel" be performed "through the data line." '137 patent at claims 10, 36. Defendants' construction clarifies that the ***same*** "data line" must be used to perform all three functions. Solas, on the other hand, contends that if there are two lines, where one is used only for "supplying" and "applying" for a given display pixel, and the other is used only for "detecting" for that display pixel, that those two ***different*** lines can nevertheless constitute "***the*** data line" of the claims. As discussed in Defendants' Opening Brief, Solas's interpretation is contrary to the plain language of the claims, contrary to precedent, and was disclaimed by the applicant during prosecution. Def. Br. at 11-12; *In re Varma*, 816 F.3d 1352 (Fed. Cir. 2016).

Solas argues, "[t]he specification gives examples of one or more data lines, and never limits ***the system*** to a single data line." Sol. Br. at 14. Solas is correct that ***the system*** can have multiple data lines, but the ***claims*** require that certain functions occur through the same data line for any particular "display pixel." As shown in Figure 16 (cropped), there can be multiple data lines (DL). But for any given display pixel (PX, blue), each of the three claimed functions of supplying the gradation current (Idata), detecting a threshold voltage (Vpv), and applying a compensation voltage (Vpre) are performed through the same data line (DL). Likewise, every other relevant Figure shows the same data line being used for all three functions for a given display pixel, demonstrating that Defendant's construction of "same data line" is the correct one. *See* '137 patent at Figs. 1, 3, 4, 5, 8, 9 10, 11, 13, 14, 19, 26.

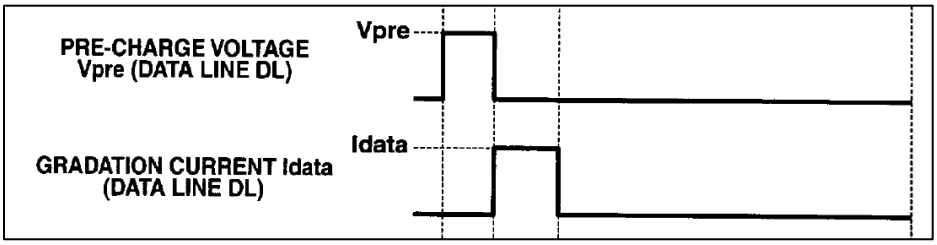


E. "before" (claim 10) and "after" (claim 36)

The claims require a particular order of events: applying a compensation voltage "before"

applying a gradation current (claim 10) or, in other words, applying the gradation current "after" the compensation voltage (claim 36). Solas acts as if it cannot understand the parties' dispute over the "common English words" before and after, and needs Defendants to "further explain" their position. Sol. Br. at 15. This is disingenuous. Solas knows what the dispute is, so much so that its expert declaration includes three pages of argument—which Solas cites without any corresponding discussion in its brief—revealing that it intends to argue "before" and "after" cover events that are "overlapping in time" rather than before or after one another. Flasck Decl. ¶ 88. Thus, there is plainly a dispute as to the meaning of these terms that needs to be resolved by the Court. *O2 Micro Int'l Ltd. v. Beyond Innov. Tech. Co.*, Ltd., 521 F.3d 1351, 1362–63 (Fed. Cir. 2008).

The only support Solas offers for its interpretation is the *ipse dixit* of its expert, who makes the conclusory assertion that the "intrinsic evidence" supports Solas's tortured position. Flasck Decl. ¶¶ 89-90. Solas's expert does not actually cite any intrinsic evidence supporting that position, and there is none. The specification teaches that applying the compensation voltage occurs earlier in time than (and not at the same time as) providing a gradation current. This is shown visually in Figure 7, which "is a timing chart showing a drive control method in the display drive apparatus." '137 patent at 8:19-20. Time is represented moving left to right, and the compensation voltage (Vpre) starts and ends entirely before the gradation current (Idata) begins.



'137 patent, Fig. 7 (cropped), 18:58-19:12 (describing Fig. 7), 21:63-64 (writing operation occurs "after the completion" of the pre-charge period), 47:40-44 (compensation voltage "immediately

before" the gradation current is supplied). That the signals are provided sequentially, and not overlapping each other, makes perfect sense in the context of the claims' separate requirement that the "compensation voltage" is applied through the same data line that the gradation current is supplied. *See supra* at Section II.D (discussing data line term); '137 patent at claims 10, 36, Fig. 7 (as shown above, labeling both signals through same "DATA LINE DL"). Because they share the same data line, the supply of the compensation voltage must start and end before the line can be used to supply the gradation current.

Solas appears to take issue with construing "before" and "after" to exclude simultaneity (i.e., "not at the same time"), but its own expert ***concedes*** that the prosecution history compels this conclusion. Specifically, Dr. Flasck acknowledges that the inventors explained to the Patent Office "that the full pla[i]n meaning of 'before' and 'after' ***obviously does not cover the situation which two things happen at the same time***." Flasck Decl. ¶ 91. This should end the inquiry.

III. U.S. PATENT NO. 7,432,891

A. "current measuring" (claims 1, 3)

The dispute over this term is by now quite familiar. The parties agree that "current" and "voltage" are different electrical concepts, yet Solas argues that it would "risk confusion" to clarify that "current measuring" means ***measuring an actual current***, and not a voltage. Sol. Br. at 17. Instead, Solas wants to leave this dispute unresolved ("[n]o construction necessary," Solas says), so it can argue to the jury that "current measuring" can be satisfied by ***voltage*** measuring. *Id.* Solas is wrong, and its position is directly refuted by the sole inventor's own statements to the Patent Office.

Specifically, to overcome the examiner's obviousness rejection based on a prior art reference by Hunter, the inventor told the Patent Office that "Hunter discloses a ***potential (or a potential***

difference) measurement,[5] but clearly ***not a current measurement***" as required by the claims. Dkt. 67-12 (Ex. 11) at 5. Likewise, the inventor emphasized that there is a "***fundamental difference between voltage and current [that] is known to anyone***." *Id.* at 4-5. Solas ignores these remarks completely, and asks the Court now to construe the claims to embrace the opposite: that the claims cover a device that measures a voltage, and that current and voltage are essentially synonymous rather than "fundamentally different."

Contemporaneous explanations and statements during patent examination, like these, are "relevant to claim construction" and can support a narrow construction even if the statements are not "so unmistakable as to be unambiguous evidence of disclaimer." *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1312 (Fed. Cir. 2017) (finding statements explaining prior art did not amount to disclaimer but supported the district court's narrow construction "for the role of claim construction is to 'capture the scope of the actual invention' that is disclosed, described, and patented.") (citations omitted). The inventor's argument here that a "potential (or a potential difference)" is "clearly not a current measurement" is highly relevant and more than enough to meet the test for disavowal. *See Saffran v. Johnson & Johnson*, 712 F.3d 549, 559 (Fed. Cir. 2013).

Solas asserts that Defendants' construction of "current measuring" is wrong simply because Defendants use the claim terms "current" and "measuring" in their construction. This is simplistic and misleading. While Defendants' construction certainly is rooted in the claim language (as it should be), it also explains that what is measured is the ***actual*** current, not a voltage—in direct contrast to Solas's effort to conflate the two distinct electrical phenomena. *Cf* Sol. Br. at 13 (claiming that "in ideal circuits, if you have one value [current or voltage], you could solve for

[5] As Dr. Holberg explains, voltage refers to potential energy, and is often used synonymously with "potential" or "potential difference." Holberg Op. Decl. ¶ 26.

the other."); *see also Leines v. Homeland Vinyl Prod., Inc.*, No. 2:18-cv-00969-KJM-DB, 2020 WL 406769, at *3 (E.D. Cal. Jan. 24, 2020) (construing "rigid material" to mean "a material that is rigid" because it would be "slightly clearer" for the jury). Solas also complains that Defendants' construction includes a negative limitation, but, as Solas points out, construing a claim term to clarify what it does not cover is appropriate when there is "specific and clear support from the intrinsic record." Sol. Br. at 18; *see also supra* at Section II.A (citing cases).

Solas's other arguments are unavailing. Solas asserts without explanation that Defendant's construction "risks ***the possibility*** of excluding the patent's preferred embodiment." Sol. Br. at 17. Of course, Solas cannot and does not argue that Defendants' construction ***actually*** would exclude the preferred embodiment, because the ***only*** thing the '891 patent describes as being measured in is a current. Indeed, as Solas admits, the "current measuring" in the patent is performed by the box U/I in the '891 patent's figure, with the "I" indicating that what is measured is a ***current***. *See id.* (showing part of the '891 patent's figure).

Solas also invokes *Linear Technology Corporation*, as if the Federal Circuit held that any claim requiring "current" cannot exclude "voltage." 566 F.3d 1049; Sol. Br. at 19. The Federal Circuit said no such thing. Instead, the court found that the specification of the patent-in-suit "expressly contemplates ***indirectly*** monitoring current ***by using a voltage measurement as a proxy***," and thus in that patent "monitoring the current to the load" could include "monitoring voltage." *Linear* at 1060. Here, Solas cannot identify any statements in the specification of the '891 patent that contemplate anything other than measuring an actual current. Moreover, unlike in *Linear*, the applicant here expressly argued to the Patent Office that the claimed current measuring does ***not*** include measuring a voltage in order to obtain the claims of the '891 patent.

B. "a third thin film transistor which during driving its gate …" (claims 1, 3)

Both parties agree that the punctuation used by the inventor in the "third thin film transistor

which during driving its gate" limitation is instructive. Sol. Br. at 16. Solas overlooks, however, that the inventor used ***semicolons*** to identify discrete limitations, and within a single limitation he identified all the acts that must occur "during driving" of the gate of the third thin film transistor: tapping, supplying, and providing. Def. Br. at 17-18; *In re Affinity Labs of Texas, LLC*, 856 F.3d 902, 907 (Fed. Cir. 2017) (finding limitations "offset by semicolons" to "strongly indicate[] that each step is separate and distinct"). Solas's argument that the "providing" step should be viewed as a wholly "separate clause and limitation" that need not occur "during driving" (Sol. Br. at 16) wars with the basic syntax and punctuation of the claim.

Solas's analysis of the claims is flawed in other respects as well. ***First,*** Solas argues that what happens "during driving" does not include the step of "providing," because the word "providing" appears several words after a comma. Sol. Br. at 16. This makes no sense logically or grammatically. The claim recites a series of things that occur "during driving" of the third thin film transistor's gate. The recitation of that series of things includes a comma connecting the "supplying" and "providing" steps, not separating them. The TFT "***supplies*** a current measuring- and voltage regulating ***circuit*** [and here is the comma:]***, said*** current measuring- and voltage regulating ***circuit providing*** to the data conductor a voltage signal …" '891 patent at 4:10-15 (claim 1).

Second, Solas ignores the third clause of the "during driving the gate" limitation, which describes that the result of the "providing step" also occurs "during driving the gate." Def. Br. at 18; '891 patent at 4:15-20. Once again, that third clause is separated by a comma, not a semicolon, and uses the definite article "***said*** current measuring and voltage regulating circuit" to refer back to the previous two uses of the term in the limitation, indicating it is part of and connected to the same limitation. *Id.*; *see Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App'x 971, 975 (Fed. Cir. 2017) ("the most natural reading of the limitation is one that incorporates all the steps

from the beginning of the attempt to access the telephone network to the end of that attempt.").

Solas argues that the ***specification*** "does not ***require*** the claimed 'providing' by the CMVR circuit to occur during driving of the transistor's gate." Sol. Br. at 17. Solas has it backwards. It is the claims, not the specification, that "define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). As discussed above, the inventor claimed that the "providing" step occurs during driving of the third transistor's gate, and Solas cannot identify any embodiment where providing ***does not*** occur during driving of the third transistor's gate. To the contrary, the specification only once discloses where the third transistor's gate is no longer driven ("switching off of the third transistor"), which follows ***after*** the "corresponding correcting signal is provided at the input of the image point circuit" (i.e., "providing to the data conductor a voltage signal") '891 patent at 2:11-18, claim 1. Furthermore, as Dr. Holberg explains, analyzing the '891 patent's only disclosed figure shows the "providing" function occurs during driving the gate of the third thin film transistor, just as recited in the claim. Holberg Op. Decl. ¶¶ 60-61 (analyzing Figure 1), ¶¶ 57-59.

Failing to find evidence for its construction in the intrinsic record, Solas cites to Defendants' IPR challenging the validity of the '891 patent to argue that Defendants purportedly "described the disputed term as two separate claim limitations." Sol. Br. at 16. Not so. In its IPR, LG Display clearly identified each of the separate and distinct limitations of claim 1 with its own letter, i.e., as a preamble [1pre] and the five limitations that follow it as [1a], [1b], [1c], [1d], and [1e]. Ex. 31 at 26-30, 33, 35, 38, 41. Directly opposite to Solas's "gotcha" argument, LG Display designated the whole of the "third thin film transistor whereby during driving its gate" limitation as a single, integrated limitation, "[1e]," just as it does here. And then, keeping with that convention, designated the three steps in limitation [e] as subparts of the same limitation by labeling them

as "[1e.1]," "[1e.2]," and "[1e.3]." *Id.* at 35, 38, 41. Of course, Solas cannot seriously argue that LG Display is setting forth a different interpretation of the claims in its IPR, as the invalidating prior art indisputably performs the "providing" step during driving the gate of the third thin film transistor as the claim language requires.

C. "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode" (claim 3)

If one were to read Solas's brief without first reading the '891 patent, one might think the patent claims that "all above mentioned elements of the driving circuit are ***physically*** located at a same side of said light emitting diode," and that Defendants were trying to read out the concept of a "physical" location in the circuit. In fact, the opposite is true. The parties ***agree*** that the phrase requires an "***electrical*** connection" of the elements of the driving circuit to the same side of said light emitting diode, and that an LED has only two sides, an anode side and a cathode side. Sol. Br. at 20. Thus, there is no dispute that the term requires an electrical connection. Rather, the dispute centers on Solas's attempt to improperly rewrite the claim language by adding two tangible, physical limitations, changing "located" to "***physically*** located" and changing "same side of said light emitting diode" to "same side ***of the layers*** of said light emitting diode."

Solas's construction is directly at odds with statements made by the applicant during prosecution and is unsupported by the specification. During prosecution, the applicant told the Patent Office that the '891 patent's disclosure of the term at issue in claim 3 is "***clearly shown in the drawings***." Dkt. 67-14 (Ex. 13) at 4. Defendants have the right to rely on such definitive statements made during prosecution regarding what the claims cover, and thus the scope of claim 3 cannot be broader than what is disclosed in the drawings of the '891 patent. *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 (Fed. Cir. 1985) ("all express representations made by or on behalf of the applicant to the examiner to induce a patent … limits the interpretation of claims").

Solas admits, however, that there is no drawing in the '891 patent that supports its attempt to read a "***physical*** location" into the claims, because the sole figure of the '891 patent "***does not depict the physical locations*** of the driving circuit elements relative to the diode." Sol. Br. at 19-21. Rather, Solas concedes that all that is disclosed in the '891 patent's figure are the "***electrical*** connections of a driving circuit," as reflected in Defendants' construction: "wherein all above mentioned elements of the driving circuit are ***electrically connected*** to the anode or cathode of said light emitting diode." Thus, Solas's attempt to "add[] language" to the claims "without support from the specification or prosecution history" must be rejected. *Source Vagabond Sys. Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1299 (Fed. Cir. 2014).

IV. U.S. PATENT NO. 7,573,068

A. "formed on said plurality of supply lines along said plurality of supply lines" (claim 1) / "connected to said plurality of supply lines along said plurality of supply lines" (claim 13)

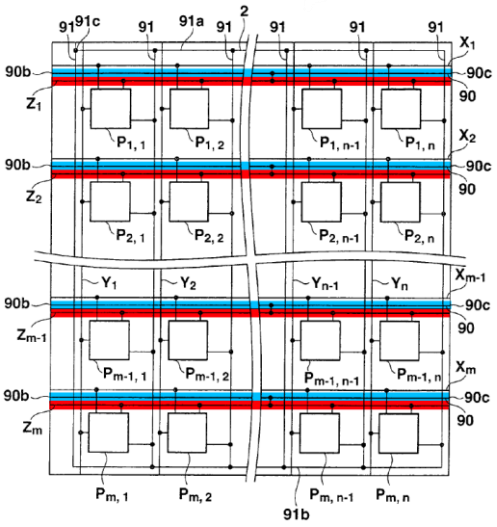
The parties agree that "along" means at least "over the length of." The dispute is whether "along" also should include "at an arbitrary point," which is what Solas apparently intends to argue to the jury if it wins its construction of "over the length or direction of."[6] As discussed below, Solas's construction would render the term "along said plurality of supply lines" superfluous, and it disregards the specification's on-point descriptions of the invention.

The parties agree that "feed interconnections" and "supply lines" are physical elements in the claimed circuit. Sol. Br. at 23. If the claims merely required one physical element to be "formed on" or "connected to" another physical element, then Solas's argument that the claims encompass "at an arbitrary point" might hold water. But that is not what the claims say. They

[6] After Defendants filed their opening claim construction brief, Solas served "first amended infringement contentions" that expose Solas's true intent to read the claim term "along" to mean "at merely an arbitrary point." Ex. 32 at 14-15 (claim 1), 47-48 (claim 13).

require one physical element to be "formed on" ***and "along"*** a second element, or "connected to" ***and "along"*** the second element. '068 patent at claims 1, 13. Thus, for feed interconnections to be "formed on" and "along" the supply lines, they must be both—but Solas's "arbitrary point" interpretation would improperly render the word "along" superfluous. *See, e.g., Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 709 F.3d 1348, 1356-57 (Fed. Cir. 2013) (rejecting construction that would render another limitation "superfluous"); *Cat Tech. LLC v. Tube Master, Inc.*, 528 F.3d 871, 885 (Fed. Cir. 2008) (refusing to adopt a construction that would render a limitation meaningless). Only Defendants' construction gives "along said plurality of supply lines" its accurate meaning of over the length of said plurality of supply lines.[7]

In "one example of the overall arrangement of the display panel," the specification describes feed interconnections "provided '***in parallel to***' the supply lines." Sol. Br. at 22, citing '068 patent at 6:26 [sic: 6:2-6]. Solas argues that this disclosure, which is in reference to Figure 1, describes feed interconnections that are "formed on or connected to the supply lines ***at particular locations***." Sol. Br. at 23. Solas is wrong. As Figure 1 shows, this arrangement of feed interconnections (blue) shows a contiguous connection over the length of the supply lines (red)—not a connection just at "particular locations."



Solas disregards the purpose of the invention: to provide reduced resistance for current to

[7] Solas's arguments concerning a lack of disclaimer or disavowal in the prosecution history miss the point. *See, e.g.*, Sol. Br. at 24. Defendants' construction of "along" aligns with, and does not depart from, its ordinary meaning—in other words, the Court does not need to find disavowal in order to give "along" its ordinary meaning. Def. Br. at 22 (dictionary definitions).

flow to a pixel, minimizing voltage drops and signal delays. *See* '068 patent at 2:5-14, 3:61-4:14. As explained by Dr. Holberg, this objective is achieved in the '068 patent by positioning the feed interconnections over the length of the supply lines (either in parallel or over a series of intersections), as reflected in every embodiment. Def Br. at 22-24; Holberg Op. Decl. ¶¶74-79. Solas's out-of-context interpretation of "along" as meaning "an arbitrary point" has no support because the resistance of the supply line would be unaffected in such a configuration, contradicting the stated objective of suppressing voltage drops and signal delays. Holberg Op. Decl. ¶ 87; *see also id.* ¶¶ 80-87 (analyzing how "feed interconnections" in the '068 patent are used to reduce the resistance of supply lines and improve voltage drop and signal delay); *see Advanced Fiber Techs. (AFT) Tr. v. J & L Fiber Servs.*, Inc., 674 F.3d 1365, 1374–75 (Fed. Cir. 2012) (reversing construction that was based on extrinsic evidence that contradicted the intrinsic evidence of record).

B. "patterned together" (claims 1 and 13)

Solas's constructions of "patterned" (formed in one or more layers) and "patterned together" (patterned to fit together) are divorced from those terms' plain meanings, and would encompass structures formed in different layers at different times, without any support in the intrinsic record. By contrast, Defendants' constructions are rooted in the specification and the context it provides about circuit manufacturing, and are amply supported by Dr. Holberg's fact-based expert conclusions as reflected in a textbook he coauthored years before the '137 patent was filed.

1. Solas's Construction of "Patterned" Is Inconsistent with Its Ordinary Meaning.

The plain, textbook meaning of "patterned" in this context refers to well-established semiconductor manufacturing steps, including deposition, photolithography and etching, used to form the components and lines of a circuit. Def. Br. at 25. The specification uses the term "patterned" in exactly this way, and makes clear that "patterning" refers to forming lines or components in a

single layer or film. *Id.* Solas's "one or more layers" construction is at odds with this ordinary meaning and the specification.

First, Solas argues that the specification discloses a "drain layer" that is formed from "two or more layers." Sol. Br. at 25. This is wrong; the surrounding context of the very sentence Solas relies on explains that the drain layer is formed in its own, single conductive film (i.e., layer):

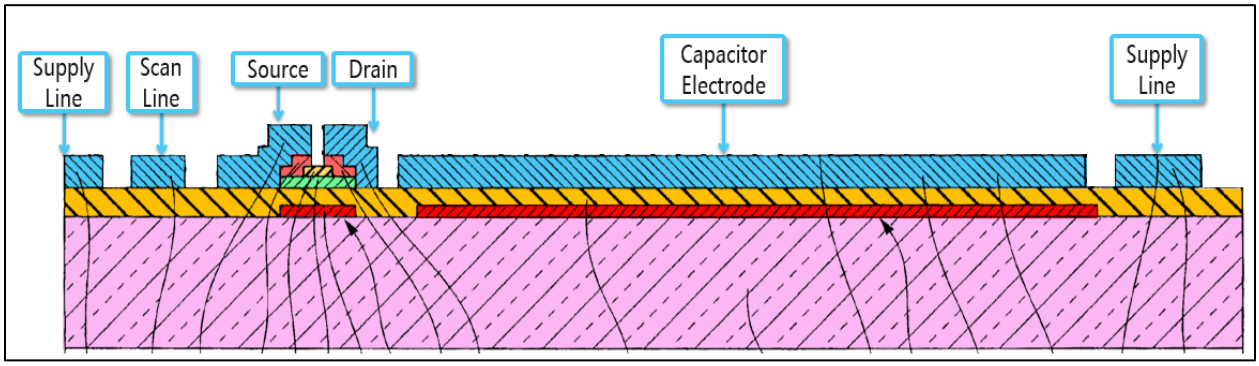
> As shown in FIGS. 5 to 8 and 10, the drains 21 d and sources 21 s of the switch transistors 21, the drains 22 d and sources 22 s of the holding transistors 22, the ***drains 23 d and sources 23 s of the driving transistors 23***, and the lower electrodes 24A of the capacitors 24 of the pixel circuits P1,1 to Pm,n, the scan lines X1 to Xm, ***and the supply lines*** Z1 to Zm ***are formed, using photolithography and etching, by patterning a single conductive film*** formed on the entire surface of the gate insulating film 31. ***The conductive film as the base of*** the drains 21 d and sources 21 s of the switch transistors 21, the drains 22 d and sources 22 s of the holding transistors 22, ***the drains 23 d and sources 23 s of the driving transistors 23,*** the electrodes 24A of the capacitors 24, the scan lines X1 to Xm, ***and the supply lines Z1 to Zm will be referred to as a drain layer hereinafter***.

'068 patent at 9:36-49; *see* Sol. Br. at 25 (citing 9:44-49).[8] Solas only cites the second sentence of this paragraph because the first sentence dooms its construction. That first sentence says the drains, sources, and supply lines are "formed, using photolithography and etching, ***by patterning a single conductive film***." '068 patent, 9:36-44. The second sentence, which Solas selectively tries to rely on, refers back to the "single conductive film" containing the drains, sources and supply lines, to be "referred to as a drain layer hereinafter." *Id.* at 9:44-49. Solas's remaining citations to a "drain layer" all refer back to this same "single conductive film." *See* Sol. Br. at 25.

Second, other parts of the specification that Solas ignores also refute its construction. Figures 5 to 8 depict the sources, drains, and supply lines being formed in a single layer. Following convention, the figures in the specification apply a uniform style of cross-hatching for each distinct

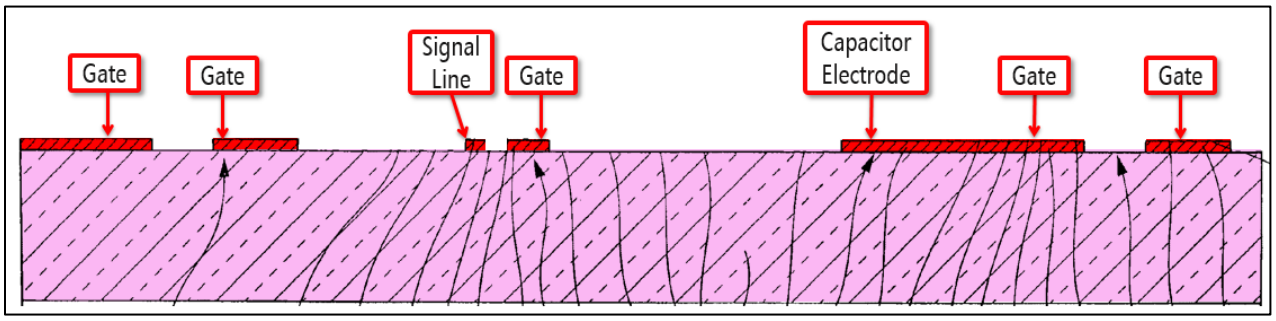
[8] Solas incorrectly states that the "drain layer" structure "includes drain 22d and source ***22c***." Sol. Br. at 25. The source is element "***22s***" and shown in Figure 8, cited by Solas (*id.*) and also shown below, to be patterned with the same conductive film (same layer) as drain 22d.

layer. This is shown, for example, in annotated Figure 8 below, wherein Dr. Holberg shows the single "drain layer" (blue) comprising the sources, drains, capacitors, supply lines and scan lines:



Holberg Op. Decl. ¶ 111 (cropping and annotating '068 patent Fig. 8); *see also id.* ¶ 110 (showing similar annotation of Figure 5), ¶ 112.

The specification similarly describes the claimed "signal lines patterned together with the gates" of the drive transistors in a single conductive film with other components as the "gate layer." *See* '068 patent claim 1, 13, 9:18-28, 14:22-27. This is shown, for example, in Figure 5 below, which shows the "signal lines," "gates" and other elements in the single layer (red).



Holberg Op. Decl. ¶ 104 (cropping and annotating '068 patent Fig. 5); *see also id.* ¶ 105. As the specification makes clear, "patterned" refers to forming components in a single layer—and not "one or more layers" as Solas argues. *See also* '068 patent at 14:17-15:40 (discussing formation of components in other layers); Holberg Op. Decl. ¶¶ 93, 103-114 (annotating figures to show components formed in each layer by patterning).

Finally, Solas points to the conclusory testimony of its expert and two prior art patents for the idea that multiple layers can be patterned in a "stack" to form a single component. Sol. Br. at 24-25. This has no bearing on the '068 patent's claims, which refer to pluralities of components that are "patterned together," not a component formed from stacked layers. '068 patent at claims 1, 13. Moreover, even if Solas's extrinsic evidence did suggest some other broader uses of "patterned," it cannot overcome the clear disclosures in the specification that this term refers to forming in a single layer. *See Choon's Design, LLC v. Idea Vill. Prods. Corp.*, 776 F. App'x 691, 696 (Fed. Cir. 2019) (rejecting patentee's attempts to broaden claim term using extrinsic evidence).

2. Solas's Construction of "Patterned Together" Violates Basic Claim Construction Principles.

In construing "patterned together" as "patterned ***to fit*** together," Solas fails to "look to the words" of claims 1 and 13 and try to explain them, and instead adds words and introduces a concept of "fitting" that changes the meaning entirely. *Vitronics*, 90 F.3d at 1582 ("we look to the words of the claims themselves . . . to define the scope of the patented invention"); *Source Vagabond*, 753 F.3d at 1299 ("Source added words to the actual claim language, thus changing the relevant comparison … [and] altering otherwise unambiguous claim language, a practice this Court has repeatedly rejected."). In contrast, Defendants' construction, which is "patterned at the same time," finds ample support in the intrinsic and extrinsic evidence and clarifies for the jury that in semiconductor manufacturing, elements that are "patterned together" are formed in a single layer, at the same time.

Independent claims 1 and 13 have identical limitations using the disputed term in two ways, describing (1) signal lines "patterned together" with the gates of driving transistors and (2) supply lines "patterned together" with the sources and drains of driving transistors. The dispute is whether

"patterned together" refers to patterning components at the same time as Defendants have explained (Def. Br. at 26-27), or whether it includes components formed in different layers, at different times, simply because they all "fit" in a device as Solas argues. Sol. Br. at 26-27.

The claim language itself refutes Solas's construction and supports Defendants'. The use of "together" in the claims reflects nothing more than the conventional, customary meaning of "together" in English, "at the same time," as confirmed by even Solas's own cited dictionaries. *See* Ex. 35 (www.dictionary.com) ("together: 6 at the same time: simultaneously"); Dkt. 68-9 at 5 (www.merriam-webster.com) ("together: 3a: at one time : simultaneously events that happened together"); Sol. Br. at 26-27 (citing same online dictionaries). Nothing in the claim language supports Solas's theory that "together" describes a future "spatial" orientation in which separate parts can be made at different times and "will fit together" later. *See* Sol. Br. at 26. To the contrary, the claims recite signal lines "patterned together" with gates, and supply lines "patterned together" with sources and drains, meaning they are fabricated at the same time in the same layer (as shown in the single layer in Figs. 5 and 8, *supra* at 23). Nothing in the claim language requires any "fitting" or an undefined future "spatial" relationship.

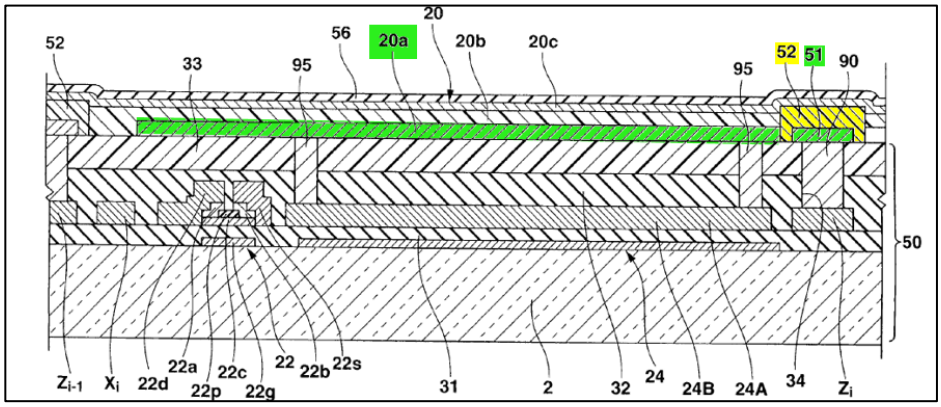
While Solas's concept of "fitting" appears nowhere in the intrinsic record—and there is not a single reference in the patent to "patterning" having anything to do with "fitting together"—Defendant's construction is taken directly from the specification. *See, e.g.,* '068 patent, 1:63-2:1 (TFT electrodes and interconnects like supply lines are formed "***at the same time***"), 1:57-62 ("***patterned simultaneously***"), 25:4-10 ("gates" and "signal lines" are "***simultaneously formed***, using photolithography and etching, by patterning a conductive film"). Indeed, every relevant figure shows the supply lines (Z_1 to $Z_{m)}$ formed at the same time (in the same layer) as the sources and drains of the drive transistors (23s and 23d), and the signal lines (Y_1 to Y_n) formed in the same

layer as the gates of the driving transistor (23g). *Id.* at Figs. 5, 6, 7, 8, 23, 24, 25.

Further supporting Defendants' construction, the specification describes one patterned film of Figure 8 as follows: "The conductive lines 51 are ***patterned together with*** the pixel electrodes 20a ***by etching a conductive film*** as the prospective pixel electrodes 20a." '068 patent at 11:11–14. Leaning heavily on the word "prospective," Solas argues that this passage somehow refutes Defendant's construction and allegedly describes patterning the conductive lines only together with "prospective pixel electrodes" in a first step, to be followed by some additional patterning of "actual pixel electrodes" in a future, undisclosed step. Sol. Br. at 27. The specification says nothing of the sort. Rather, it is unambiguous that what is "patterned together" are "conductive lines 51" and "pixel electrodes 20a," and that the ***un-etched*** (and so un-patterned) "conductive film" makes up "the prospective pixel electrodes 20a," but when that film is "***patterned … by etching***" the finished electrodes and the conductive lines have been "patterned together." '068 patent at 11:1-14; *see also id.* at 1:63-67 (manufacturing "a conductive thin film as a prospective electrode of a thin-film transistor is subjected to photolithography and etching to form the electrode"), 25:18-20, 26:40-43; Ex. 28 ("Holberg Resp. Decl.") ¶¶ 7-15 (describing use of "prospective" in the '068 patent). This is entirely aligned with Defendants' construction.

Figure 8 removes any doubt that "conductive lines 51 patterned together with the pixel electrodes 20a" refers to patterning at the same time, and cannot mean patterning them "to fit" together as Solas proposes. As shown below, the pixel electrode 20a and conductive lines 51 are patterned from the same "transparent conductive film" (green), and therefore necessarily made in the same patterning step, at the same time. '068 patent at 11:4-11; Holberg Resp. Decl. ¶ 9. Indeed, fatal to Solas's argument, this figure confirms that the pixel electrodes 20a and conductive lines 51 do not "fit together" at all; they are separated from each other by an "insulating film 52"

(yellow). *Id.* at 11:18-27; *see also id.* at 26:43-47.



'068 patent at Fig. 8 (annotated); Holberg Resp. Decl. ¶ 9.

Perhaps realizing that its position is untenable, Solas proposes an alternative construction, arguing that Defendants' construction could be adopted and broadened to include "sequential" patterning, not just patterning at the same time. Sol. Br. at 27. The Court may reject this outright, as Solas never disclosed this construction in compliance with the Court's scheduling order, and this new, barebones contention is insufficient to preserve the argument. *See Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1250 n.2 (Fed. Cir. 2008). Even on the substance, Solas's alternative construction fails, for Solas offers no evidentiary support for it—nothing from the claim language, specification, file history, or anything else. As explained above, all of the reliable evidence establishes that the relevant patterning is at the same time in a single layer, not sequentially.

C. "signal lines" (claims 1 and 13)

Solas's proposed construction of "signal lines" again fails to consider the context in which the term is used. ***First,*** Solas ignores that different claim terms are presumed to have different meanings. *CAE*, 224 F.3d at 1317. If "signal lines" mean any "conductive lines carrying a signal," as Solas argues, then they would not have a meaning different from any of the other lines recited in the claims, including "supply lines," which the parties agree should be construed as "conductive lines carrying a current or voltage." Dkt. 67-28 (Ex. 27) at 3; '068 patent at claims 1, 13. ***Second,***

Solas points to nothing in the specification to supports its proposed construction. *Phillips*, 415 F.3d at 1321 ("the specification is the single best guide to the meaning of a disputed term").

The specification explains exactly what "signal lines" are in the context of "conventional" OLED panels: "conductive lines supplying a value corresponding to a luminance level." '068 patent at 1:34-36; *see also id.* at 19:17-19, 25:10-12. This differentiates them from "supply lines," which supply the current or voltage used to illuminates the OLED, and also from "scan lines," which carry on/off "shift pulses" to select a pixel. Def. Br. at 27-28.

Solas argues that Defendants' construction should be rejected because it reflects a concept of "luminance" described only in the background of the invention. That is not correct, and Solas's myopic focus on the word "luminance" is misplaced. The '068 patent uses "luminance" interchangeably with "gray level" throughout the specification to refer to the brightness level of the display pixel. *See, e.g., id.* at 19:17-19 ("***the highest luminance gray level*** (brightest display)"), 19:19-24 ("luminance gray level between the highest luminance gray level and the lowest luminance gray level"); 19:31-32, 19:61-62, 19:66, 20:6-7, 20:21. The specification then describes the operation of its "signal lines" as providing a value corresponding to a display gray level (i.e., luminance level), distinguishing them from supply lines and scan lines. '068 patent at 25:10-12 ("signal lines Y1 to Yn are interconnections to which a . . . ***value corresponding to the display gray level flows***."), 16:14-34, 17:19-40, 19:19-23, 19:31-46, 19:61-67, 20:5-7, 20:19-22, 30:30-51 (references to "luminance gray level" supplied from "signal lines"), Figs. 2, 21; *cf id.* at 15:38-60 (supply line applies a "write feed voltage"), 16:48-55 (supply line supplies a "driving feed voltage" and "driving current"), 16:5-8 (scan lines applies a "shift pulse"), 16:65-17:5 (same), 17:11-13 (same). Defendants' construction, which follows the inventors' "repeated[] and consistent[]" description of the signal lines should be adopted. *Wi-LAN USA, Inc. v. Apple Inc.*, 830 F.3d 1374,

1382 (Fed. Cir. 2016) ("[T]he specification's consistent references to multiple 'specified connections' [] weigh in favor of a construction excluding embodiments where the intermediary node is capable of maintaining only one 'specified connection.'"); *Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1318 (Fed. Cir. 2014) ("The fact that anonymity is ***repeatedly and consistently*** used to characterize the invention strongly suggests that it should be read as part of the claim.").

D. "feed interconnections" (claims 1, 10, 12, 13, 17)

Once again, Solas fails to point to any support in the specification for its construction. Instead, Solas argues that the specification does not clearly and unambiguously disclaim the "plain meaning" of "feed interconnections" that it purportedly proposes. Sol. Br. at 29. The problem for Solas, even adopting its misunderstanding of the law[9], is that the unique, coined, technical term "feed interconnections" has no ordinary meaning to disclaim. It is not a term of art, and there are no pertinent general or technical dictionary definitions. Holberg Op. Decl. ¶ 119. Thus, following *Phillips*, we turn to the specification for guidance on its meaning. *Phillips*, 415 F.3d at 1315 (the specification "is the single best guide to the meaning of a disputed term"). Indeed, such "[i]diosyncratic language, highly technical terms, or terms coined by the inventor are best understood by reference to the specification." *3M Innovative Properties Co. v. Tredegar Corp.*, 725 F.3d

[9] *Phillips* does not hold that the specification is only relevant if it sets forth an express definition or disclaims some known plain meaning of a term. On the contrary, the *en banc* Federal Circuit squarely rejects this principle when it reverses the holding in the *Texas Digital* case and its progeny. *Phillips*, 415 F.3d at 1320 ("Although the concern expressed by the court in *Texas Digital* was valid, the methodology it adopted placed too much reliance on extrinsic sources such as dictionaries, treatises, and encyclopedias and too little on intrinsic sources, in particular the specification and prosecution history."); *id.* at 1321 ("Assigning such a limited role to the specification, and in particular requiring that any definition of claim language in the specification be express, is inconsistent with our rulings that the specification is 'the single best guide to the meaning of a disputed term,' and that the specification 'acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.'"); *id.* at 1315 ("claims must be read in view of the specification, of which they are a part.") (citation and internal quotation marks omitted).

1315, 1321 (Fed. Cir. 2013); *accord Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1287 (Fed. Cir. 2010); *MyMail, Ltd. v. Am. Online, Inc.*, 476 F.3d 1372, 1376 (Fed. Cir. 2007).

The specification resolves the dispute and confirms that Defendants' construction (which clarifies that the feed interconnections are conductive layers different from the gates, sources, and drains) is correct. No fewer than ten times, the specification explains that the feed interconnections are formed separately from the "gate, sources and drains": once in the "Summary of the Invention," twice in the detailed description, and in all seven figures depicting the feed interconnections as formed separately from the gates, sources and drains. '068 patent at 3:61-64, 18:30-33, 21:61-66, Figs. 5, 6, 7, 8, 23, 24, 25. The specification emphasizes that by forming the feed interconnections differently from the gates, sources and drains, the inventors solved the voltage drop problem that arises when interconnects are formed with them. '068 patent at 18:32-39, 2:38-41; *cf id.* at 18:26-29 (describing layers with the "gate or the source/drain" have "too high" a resistance), 2:5-35.

Solas has presented no evidence of a contrary meaning, and indeed does not cite any intrinsic evidence in support of its broad construction, only attorney argument.[10] Solas also cites to its expert, but Dr. Flasck's declaration simply parrots the same "conclusory, unsupported assertions" as Solas's brief which is "not useful to a court," *Phillips*, 415 F.3d at 1318, and deserves no weight. *See SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1210 (Fed Cir. 2013).

V. CONCLUSION

For the reasons explained above, Defendants respectfully request that the Court issue an order adopting their proposed constructions of the disputed claim terms.

[10] Solas contends Defendant's construction may "create some confusion" regarding what provides the connections, the feed interconnections or the gates, sources and drains. Sol. Br. at 30. To avoid any possible confusion, Defendants would have no objection to a construction adding the following highlighted commas: "conductive structures, in a layer or layers different from the gates, sources and drains, that provide connections to a source that supplies voltage and/or current."

Respectfully Submitted

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CERTIFICATE OF SERVICE

The undersigned certifies that on the 3rd day of April, 2020, I electronically filed this document with the Clerk of Court via the Court's CM/ECF system which will send notification of such filing to all counsel of record, all of whom have consented to electronic service in this action.

/s/ Jennifer H. Doan
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